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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,885	10/02/2003	Sau C. Wong	M8450US1C	2319

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PATENT LAW OFFICES OF DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120

EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/678,885	**Applicant(s)** WONG, SAU C.	
	Examiner Jasmine Song	**Art Unit** 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

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Detailed Action

1. This office action is in response to Amendment filed on 12/20/2004. Claims 1-20 are pending in the application. All rejections and objections not explicitly repeated below are withdrawn.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

3. The rejection of claims 1-20 has been maintained and updated as shown below.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yard et al., U.S. Patent 5,896,393, in view of Hazen., U.S. Patent 5,379,413.

Regarding claim 1, Yard teaches that a method for operating a semiconductor memory, comprising:

storing at least a portion of each of a plurality of data blocks in a physical array (col.4, lines 47-49, a physical array is taught as a storage array, col.4, lines 38-42) in the memory (the memory is taught as the flash memory array 12 as shown in Fig.1)

selecting one or more of the data blocks for erasure (it is taught as the deleted files within the storage array, col.4, lines 59-60 and col.5, lines 3-5);

reading first data from the physical array, wherein the first data comprises all data from blocks other than the data blocks selected for erasure is taught as copying only the active files within the storage array to the update array (col.5, lines 7-10);

Yard does not teach erasing the entire physical array wherein erasing begins after reading the first data and writing the first data back into the physical array after erasing the entire physical array. Yard teaches that erasing the storage array sectors (col.5, lines 9-10) and the reassigned storage array will begin at the first array location of the first active file (col.5, lines 15-17). In other words, the difference between the invention and the Yard's reference is: the current invention claims that erasing the entire physical array and writing the first data back into the physical array after erasing the entire physical array, however, the Yard discloses that erasing the storage array sectors during the update procedure (see Fig.1A, after step 208, the process goes back to step 202, also see col.7, lines 33-39)

However, Hazen teaches erasing the entire physical array, wherein erasing begins after reading the first data (it is taught as the first data must be saved before erasure occurs, col.1, lines 42) and writing the first data back into the physical array after erasing the entire physical array (col.1, lines 40-44).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Hazen such as erasing the entire physical array and writing the first data back into the physical array after erasing the entire physical array because the repeat number of erase operations for memory cells can be minimized to shorten the erase verify processing time. Since the repeat number of erase operations is minimized, over erasing of memory cells can be suppressed, the number of memory cells depleted at the end of erase processing can be reduced, and the processing time of subsequent write-back processing can be shortened. This can shorten the total processing time of the wafer inspection step, can improve the productivity of the nonvolatile semiconductor memory device, and can reduce the manufacturing cost. Moreover, since the numbers of erase and write-back processes decrease deterioration of the gate oxide film can be prevented so as not to degrade the electron holding characteristic of the floating gate and erase any memory data. Consequently, the reliability of the flash memory can be maintained.

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 2, Yard teaches storing the first data in temporary storage while erasing the physical array is taught as copying the active files to the update array (col.5, lines 8-9 and col.7, lines 36-37), wherein the temporary storage is external to the semiconductor memory.

Regarding claim 3, Yard teaches that erasing the physical array comprises simultaneously erasing all memory cells in the physical array (col.2, lines14-16 and col.4, lines 67 to col.5, lines 2).

Regarding claim 4, Yard teaches that the physical array is partitioned into a plurality of separately erasable sectors (col. 2, lines 16-19 and col.3, lines 31-33), and erasing the entire physical array comprises erasing all of the sectors (col. 5, lines 9-10).

Regarding claim 5, Yard teaches that the sectors are sequentially erased is taught as each sector may be individually erased (col.5, lines 33-34).

Regarding claim 6, Yard teaches that the writing comprises writing data from different data blocks at consecutive addresses in the physical array without regard for boundaries between sectors is taught as writing back the active data files into the storage array from the first array location of the first active file of the update array (col.5, lines 15-17).

Regarding claim 7, Yard teaches further comprises writing data from one or more new data blocks into the erased physical array is taught as reassigning the active files stored in the update array into storage array (col.5, lines 15-17).

Regarding claim 8, Yard teaches that the memory is a Flash memory (the background of the invention).

Regarding claim 9, Yard teaches that the physical array contains multi-bit-per-cell memory cells which is the conventional in the flash memory art.

Regarding claim 10, Yard teaches reading data from at least a portion of the physical array (read active files from the storage array), comprises reading all data stored in the physical array, including second data that is the one or more data blocks selected for erasure (col.7, lines 56 to col.8, lines 3).

Regarding claim 11, Yard teaches maintaining a count indicating a number of erase operations performed on the physical array (col.4, lines 28-30 and col.7, lines 46 to col.8, lines 17); and

selecting parameters for operation of the physical array, the parameters being selected according to the count (col.1, lines 26-61 and col.8, lines 13-17).

Regarding claim 12, Yard teaches that a system for storage of data blocks, comprising:

a first memory that is a non-volatile semiconductor memory is taught as a flash memory array (Fig.1); and

a compute system (col.4, lines 26-27) connected to the first memory, the compute system comprising a storage device (Fig.1); and

a processor (col.4, lines 28 and col.10, lines 32) that executes file management procedure (col.4, lines 23-46), wherein execution of the file management procedure comprises:

identifying a plurality of data blocks at least partly stored in an array in the first memory, selecting one or more of the data block for erasure (col.4, lines 47-60);

reading from the array data corresponding to all of the data blocks that are not selected for erasure (col.5, lines 7-10);

storing in the storage device (col.5, lines 7-10), the data read from the selected array;

Yard does not teach erasing the entire physical array wherein erasing begins after reading the first data and writing the first data back into the physical array after erasing the entire physical array. Yard teaches that erasing the storage array sectors (col.5, lines 9-10) and the reassigned storage array will begin at the first array location of the first active file (col.5, lines 15-17). In other words, the difference between the invention and the Yard's reference is: the current invention claims that erasing the entire physical array and writing the first data back into the physical array after erasing the entire physical array, however, the Yard discloses that erasing the storage array sectors during the update procedure (see Fig.1A, after step 208, the process goes back to step 202, also see col.7, lines 33-39)

However, Hazen teaches erasing the entire physical array, wherein erasing begins after reading the first data (it is taught as the first data must be saved before erasure occurs, col.1, lines 42) and writing the first data back into the physical array after erasing the entire physical array (col.1, lines 40-44).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Hazen such as erasing the entire physical array and writing the first data back into the physical array after erasing the entire physical array because the repeat number of erase operations for memory cells can be minimized to shorten the erase verify processing time. Since the repeat number of erase operations is minimized, over erasing of memory cells can be suppressed, the number of memory cells depleted at the end of erase processing can be reduced, and the processing time of subsequent write-back processing can be shortened. This can shorten the total processing time of the wafer inspection step, can improve the productivity of the nonvolatile semiconductor memory device, and can reduce the manufacturing cost. Moreover, since the numbers of erase and write-back processes decrease deterioration of the gate oxide film can be prevented so as not to degrade the electron holding characteristic of the floating gate and erase any memory data. Consequently, the reliability of the flash memory can be maintained.

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 13, yard teaches that the data blocks are files representing music, and the first memory is a memory in a player of the music (col.2, 1-9).

Regarding claim 14, Yard teaches that the computer system is a personal computer (Fig.1).

Regarding claim 15, Yard teaches that the file management procedure writes the data blocks from the storage device back into the erased array (col.5, lines 15-17).

Regarding claim 16, Yard teaches that the file management procedure further comprises writing new data into erased array (col.5, lines 15-17).

Regarding claim 17, Yard teaches that erasing the array comprises simultaneously erasing all memory cells in the array (col.2, lines 14-16).

Regarding claim 18, Yard teaches that the array is partitioned into a plurality of separately erasable sectors, and erasing the array comprises erasing all of the sectors (col.2, lines 18-19 and col.3, lines 31-33).

Regarding claim 19, Yard teaches that the sectors are sequentially erased (col.5, lines 33-34).

Regarding claim 20, Yard teaches that the writing comprising writing data from different data blocks at consecutive addresses in the array, without regard for boundaries between the sectors (col.7, lines 46-51).

Response to Applicants' Arguments

6. Applicant's arguments filed 12/20/2004 have been fully considered but they are not persuasive.

In response to applicant's argument that Yard fails to suggest erasing the array in its entirety and rewriting the data to be kept (see applicant's remarks page 6, first two lines of last paragraph), it is noted that this limitation is taught by Hazen, Hazen teaches erasing the entire physical array, wherein erasing begins after reading the first data (it is taught as the first data must be saved before erasure occurs, col.1, lines 42) and writing the first data back into the physical array after erasing the entire physical array (col.1, lines 40-44). Please refer back to the rejections as shown above.

In response to applicant's argument that Hazen fails to suggest modification of Yard because Hazen is not directed to file management system or erasing an entire array in multi-sector system such as Yard (see applicant's remarks page 6, last three lines of last paragraph and last two lines of page 5 to first two lines of page 6), it is noted that the applicant admitted that Hazen teaches a multi-sector flash memory since all the memory cells connected to a common source line (e.g., to one sector of a multi-sector flash memory) in applicant's remarks page 5, last three lines of paragraph 5.

In response to applicant's argument that Neither Yard Nor Hazen provide or suggest such this (see page 6, second paragraph, "In accordance with ... This can improve storage efficiency because data blocks can be stored without unused storage cells between data blocks) or any other motivation for modifying Yard, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-5:30 (First Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song
Patent Examiner
May 31, 2005

FoR
Mano Padmanabhan
Supervisory Patent Examiner
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Gary D Portka
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PRIMARY EXAMINER